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If the user enables the multi-bit flip flop conversion in the flow then the tool will first check the available multibit flops in the library. (You can read more about multi-bit cell here ) The tool considers the criticality of timing associated with a single bit of flop and the user constraint set for multi-bit conversion and based on the ...

### **Team VLSI**

OpenHW Group CORE-V CV32E40P RISC-V IP. CV32E40P is a small and efficient, 32-bit, in-order RISC-V core with a 4-stage pipeline that implements the RV32IM[F]C instruction set architecture, and the Xpulp custom extensions for achieving higher code density, performance, and energy efficiency [], [].It started its life as a fork of the OR10N CPU core that is based on the OpenRISC ISA.

### **GitHub - openhwgroup/cv32e40p: CV32E40P is an in-order 4 ...**

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